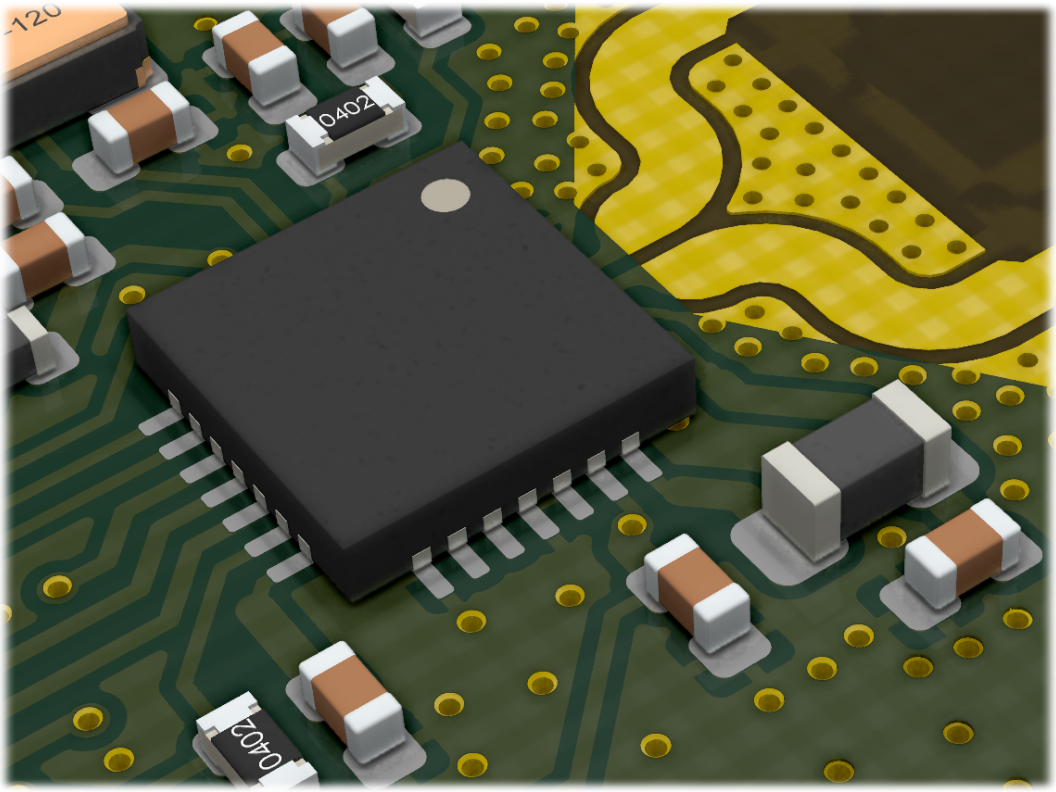
SPARK MICROSYSTEMS

SR10x0 Hardware Design Guide



Revision 1.2

Monday 28th November, 2022

Abstract

This document provides information on designing UWB applications using the SPARK Microsystems SR10x0 chipsets. It is intended for system designers and integrators who require a complete overview of the hardware implementation.

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1 Hardware System Overview

1.1 SR10x0

The SR10x0 family is composed of digitally programmable UWB wireless transceivers that work in the license-free UWB spectrum (SR1010: 3.1 - 5.8 GHz, SR1020: 6.0 - 9.3 GHz). The ASICs are composed of an impulse radio with an RF transmitter and receiver, power management unit, sleep counter and digital / baseband hardware, and a SPI interface.

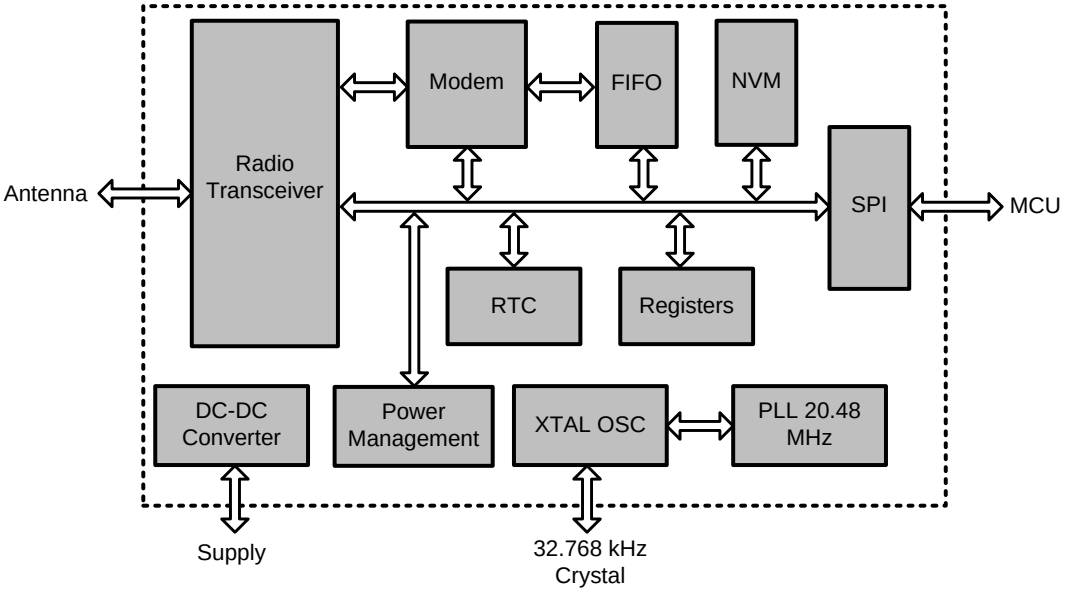


Figure 1: SR10x0 Block Diagram

1.2 System Block Diagram

A system design based on SR10x0 chipsets requires a host controller to communicate with the chipsets and implement the link layer. Several passive components are required, such as resistors, capacitors, an inductor for the internal DC-DC, a crystal oscillator and RF matching components (such as a balun and antenna). If the power source output voltage isn't within the input range of the SR10x0, a voltage regulator would also be required. An example of a simplified hardware block diagram of such system is shown in Figure 2.

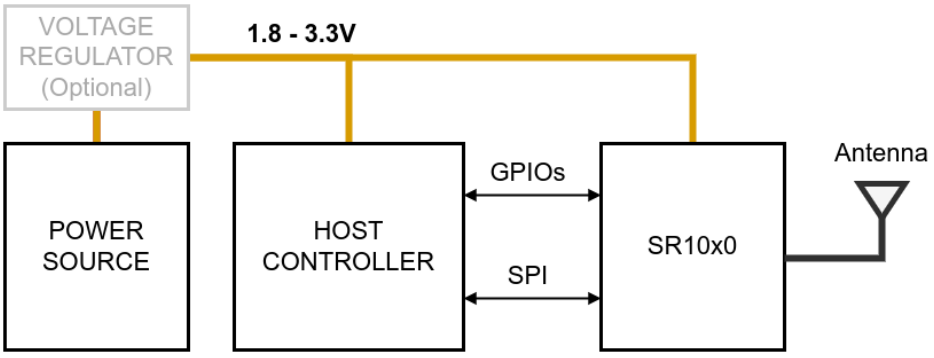


Figure 2: System Overview

1.3 Reference Circuit

The circuit schematic shown in Figure 3 could be used as a reference for the SR10x0 in a typical application. The recommended component values and part numbers are given in Table 4.

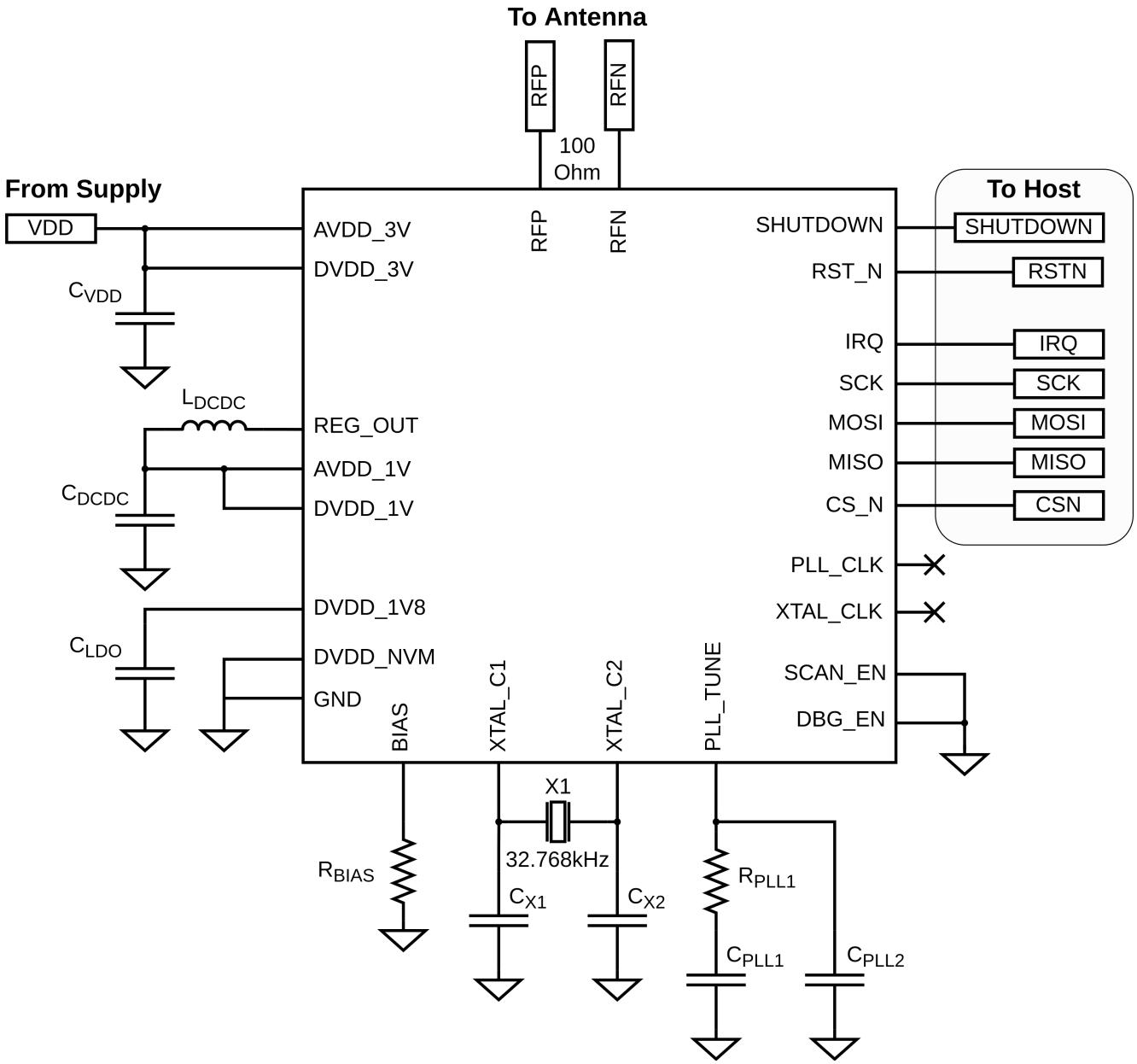


Figure 3: SR10x0 Reference Circuit

1.4 Recommended Part Values

Table 4 shows the list of recommended values.

Component	Description	Value	Package
C_{VDD}	Main supply decoupling capacitors	$2 \times 1\mu F$	Ceramic
L_{DCDC}	Internal DC-DC inductor	180nH	
C_{DCDC}	Internal DC-DC decoupling capacitor	$1\mu F$	Ceramic
C_{LDO}	Internal LDO decoupling capacitor	100nF	Ceramic
R_{BIAS}	Internal current biasing resistor	$2.2M\Omega \pm 1\%$	
X_1	Crystal oscillator	32.768KHz	
C_{X1}, C_{X2}	Crystal load capacitors	See section 2.2.1	Ceramic
R_{PLL1}	PLL filter resistor	$390k\Omega \pm 5\%$	
C_{PLL1}	PLL filter capacitor 1	680pF	Ceramic **C0G (NP0)**
C_{PLL2}	PLL filter capacitor 2	68pF	Ceramic **C0G (NP0)**

Table 4: Recommended Component List

Table 5 shows the list of recommended part numbers for the 32.768KHz crystal oscillator (X_1).

Manufacturer	Part Number	Package
Abracon	ABS07-120-32.768KHZ-T	3.2x1.5mm
Micro Crystal AG	CM7V-T1A-32.768KHZ-6PF-20PPM-TA-QC	3.2x1.5mm
ECS Inc.	ECS-.327-7-34B-TR	3.2x1.5mm
ECS Inc.	ECS-.327-6-34S-TR	3.2x1.5mm

Table 5: Recommended Part Numbers for X_1 Crystal

Table 6 shows the list of recommended part numbers for the 180nH inductor (L_{DCDC}).

Manufacturer	Part Number	Package
TDK Corporation	MLJ1608WR18JT000	0603
TDK Corporation	MLJ1005WR18JT000	0402

Table 6: Recommended Part Numbers for L_{DCDC} Inductor

2 Circuit Design Guidelines

2.1 Power

2.1.1 Main Power Supply

The main power feed of the SR10x0 needs to be free from digital noise to operate in the full specifications range. It is highly recommended to decouple the SR10x0 external supply from the rest of system. In the event where the SR10x0 shares the same system supply as other ICs, it is recommended to filter the input using a ferrite bead, as shown in Figure 7.

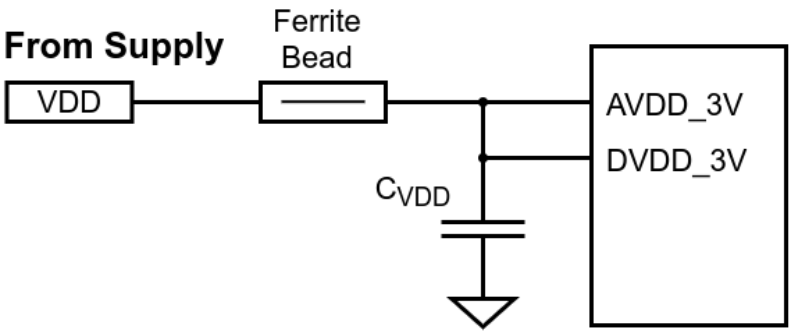


Figure 7: VDD Filter

The SR10x0 generates high-frequency noise across its specified bandwidth and therefore multiple capacitors of different values can help to maintain the decoupling impedance low throughout the frequency spectrum. In order to further reduce dependence from the generated noise, the `AVDD_3V` and `DVDD_3V` pins of the SR10x0 can each be decoupled with multiple capacitors of different values and the smaller value capacitors should be placed closest to the power pin.

Decoupling capacitors should be placed as close as possible to the power pins to minimize the inductive impedance created by the length of the traces. It is recommended to use 0603 size or smaller, low-ESR, surface mount capacitors. Larger packages will be less effective for decoupling as the parasitic inductance increases with size.

2.1.2 Internal DC-DC

The SR10x0 features an internal DC/DC converter which generates a 1V voltage on the `REG_OUT` pin which is required to be routed back into the device through the `DVDD_1V` and `AVDD_1V` pins. The `REG_OUT` pin should be connected to an LC circuit as shown in section 1.3. The external components should be placed as close as possible to the `REG_OUT` pin to minimize the inductance loop and radiation.

CAUTION

The capacitance load on the `REG_OUT` pin should be **limited to 1μF**.

The inductor L_{DCDC} connected to this pin should meet the following specifications:

- ESR $<$ 500mOhm
- Saturation current $>$ 200mA
- Self-resonance frequency $>$ 200MHz

CAUTION

The inductor's ESR value has a direct impact on the power consumption of the radio, as a higher ESR value increases the dissipated power of the regulator circuit.

For very low-power applications, SPARK Microsystems recommends that you select an inductor with the **lowest ESR value available**, while respecting the other recommended specifications.

2.1.3 Digital Supply

The `DVDD_1V8` pin should be decoupled externally using a 100nF capacitor, and should not be used for any other purpose. The decoupling capacitor should be placed as close as possible to the `DVDD_1V8` pin to minimize the inductive impedance created by the length of the traces.

2.1.4 NVM

The `DVDD_NVM` pin is used for factory programming calibration data into the Non-Volatile Memory (NVM) and should be connected to GND for all applications.

2.1.5 BIAS

The `BIAS` pin is used as a internal current reference. Connect this pin to a 2.2MΩ $\pm$1% resistor.

2.2 Clock

2.2.1 Crystal Oscillator

The SR10x0 uses an external crystal oscillator to generate a 32.768kHz clock and run the Real Time Clock (RTC) circuit. This clock is also used to synthesize an on-chip 20.48MHz clock using a PLL which requires an external filter (see section 2.2.2).

Make sure to use adequate values for the load capacitors according to the selected crystal oscillator and ensure that they are placed as close as possible to the crystal pins. To find out the right capacitor value, use the following formula:

$C_{X1} = C_{X2} = 2 \times C_L - (C_{PIN} + C_{PCB})$

where:

- C_L : Crystal load capacitance (from crystal datasheet)
- C_{PIN} : SR10x0 pin capacitance (1pF)
- C_{PCB} : PCB parasitic capacitance (1-2pF range)

Combining the above formula with the specifications of the recommended Abracon crystal, the recommended load capacitor value would be:

$C_{X1} = C_{X2} = 2 \times 6 - (1 + 1) = 10pF$

2.2.2 PLL_TUNE

The external filter circuit is important for the chipset internal timing and the PLL_TUNE input **is very sensitive to noise** therefore should be isolated from noise sources. The grade for the capacitors used for the PLL filter should be **C0G (NP0)** to minimize the piezoelectricity effect and maximize stability over the temperature range.

The filter has been validated with the circuit shown in section 1.3 and the following component values:

- R_{PLL1} = 390kΩ ±5%
- C_{PLL1} = 680pF
- C_{PLL2} = 68pF

Note that the tolerance of R_{PLL1} is not critical and if resistors with larger tolerance are available, they can be used instead.

2.2.3 External Sources

When a 32.768KHz crystal is used, the XTAL_CLK and PLL_CLK pins should be left floating.

In very specific conditions, the SR10x0 can sink either the 32.768kHz crystal clock or the 20.48MHz PLL clock from an external clock signal through the XTAL_CLK and PLL_CLK pins respectively. If the 32.768kHz is sourced from an external clock signal, then the crystal oscillator is not required. Alternately, these pins could be used as outputs to monitor the internal clock signals. Please refer to the SR10x0 datasheet for more information about configuring these pins as outputs.

WARNING

PLL_CLK and XTAL_CLK pins are pulled down to ground at startup. If an external oscillator is connected to one of those pins, and if that oscillator is also used by other devices, then these might be prevented from working normally while the radio is not completely configured.

2.3 Host Interfaces

2.3.1 SPI

The SR10x0 communicates with an external host controller through a standard Serial Peripheral Interface (SPI), which supports full-duplex mode. The SPI logic voltages track the main supply of the SR10x0, therefore ensure the SPI signals from the host do not exceed the supply voltage to avoid irreversible damage. The selected host controller SPI interface should be dedicated to the radio, in other words **the radio should be the only device connected to this SPI interface**.

The CS_N (active-low chip select) pin should be connected to the host controller even if the SR10x0 is the only chip on the SPI bus, as this pin is used in the burst read/write protocol.

The IRQ (interrupt request) pin should be connected to a host controller interrupt pin in order to use the user configurable interrupt feature in the SR10x0.

Troubleshooting

SPARK Microsystems recommends to add test points on SPI and IRQ signals to facilitate probing.

2.3.2 SHUTDOWN and RST_N

The SHUTDOWN and RST_N (active-low reset) pins are used to control the power states and power sequencing of the SR10x0. For more details, refer to the SR10x0 datasheet.

Connecting the SHUTDOWN and RST_N pins to host controller GPIO pins is optional and depends on the application. If not connected to host controller GPIOs, the SHUTDOWN pin should be connected to ground, and the RST_N pin should be connected to an RC network as suggested in Figure 8.

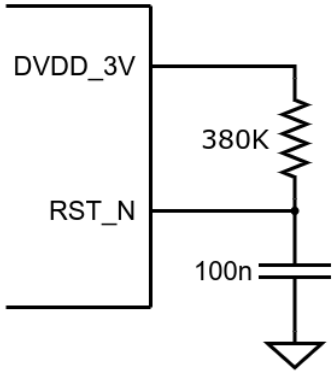


Figure 8: Reset Network

The RST_N can also be connected directly to the host controller without the need of an RC network. However, we recommend keeping a pull-up resistor on the line for situations where the host controller is not actively driving this input.

Troubleshooting

SPARK Microsystems recommends to add test points on SHUTDOWN and RST_N signals to facilitate probing.

2.3.3 SCAN_EN and DBG_EN

SCAN_EN and DBG_EN are used exclusively by SPARK Microsystems for testing and validation during production test. Connect both these inputs to ground for proper operation, as shown in section 1.3.

2.4 RF Interface

The SR10x0 chip features a balanced RF port which can be connected to a differential transmission line or can be converted to a single-ended transmission line using a balun.

For more details about the RF interface and the recommended design guidelines, refer to section 4.

For antenna design and specifications, documentation is available upon request.

3 PCB Design Guidelines

Proper component placement and layout are essential for successful implementation and to achieve the best performances.

Figure 9 shows a proper placement and layout implementation of the SR10x0 chipset and external components. The ”labelled” components are match those specified in the reference circuit shown in Figure 3. Note that the antenna shown below is specific to the SR1020 chipset.

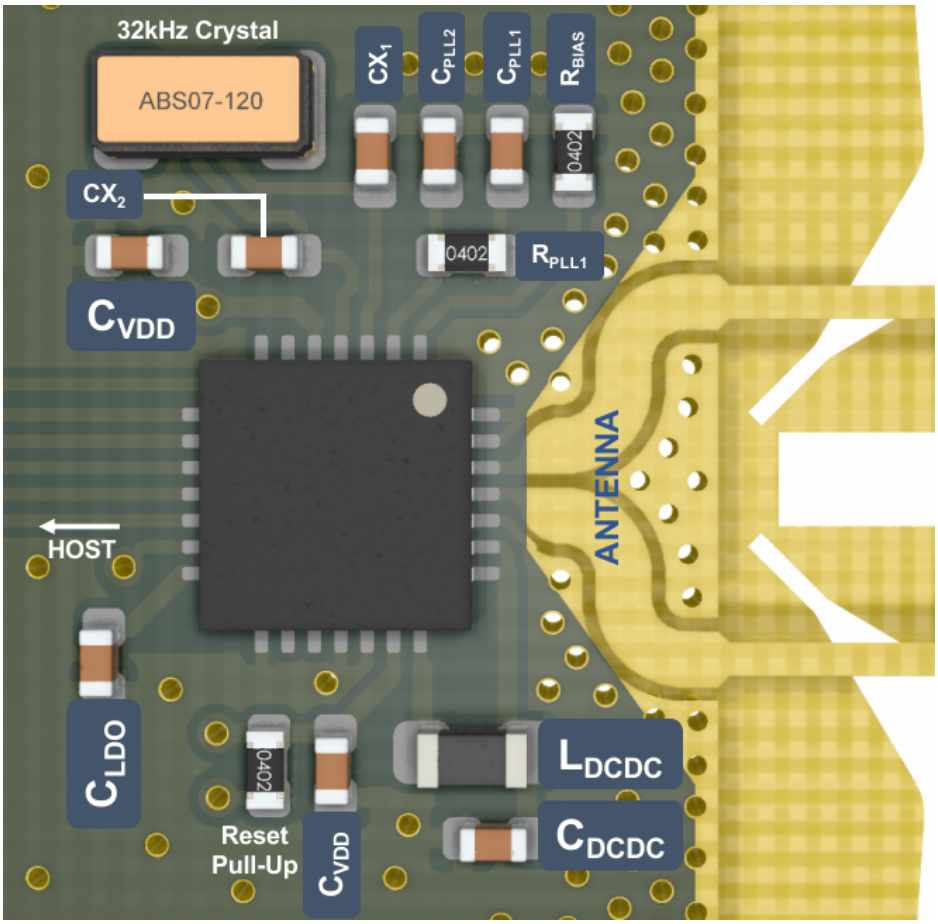


Figure 9: SR10x0 Reference Layout

3.1 Power

The SR10x0 can be powered using a 1.8V to 3.3V supply voltage. The power management section including the voltage regulators and the battery charger should ideally be placed close to the battery port and away from the noise sensitive components. This is most important when switching power circuits are used as the high switching currents will introduce both conductive and radiated noise. Proper distance and/or shielding will help minimizing the effect of the radiations on other parts of the circuit.

The best power distribution technique to minimize conductive noise is star routing. By using dedicated power routes from the power source to each system block, the RF block will get isolated from the conductive noise created by other blocks. If start routing is not possible then a series power distribution could be used with some considerations.

Power routes should be as wide as possible to minimize the inductance of the traces (power planes are preferred). Proper filtering of the power supply paths to each block also helps to minimize the effect of the generated noise from one block to the other blocks. An LC filter or ferrite beads are examples of such filtering.

Ground return paths to decoupling capacitors and IC pins should be as low impedance as possible. Use ground vias as close as possible to the ground pins and do not use long thin traces for ground connections. If more than one ground plane is used, connect the ground planes using vias at several points to minimize the ground impedance. Using 2 or more vias in parallel reduces the inductance of the vias significantly, so it is recommended to use parallel vias when connecting the ground pins of decoupling capacitors to the ground plane when possible.

If power is sourced through a via, the decoupling capacitor should be placed between the via and the power pin, to ensure that the high frequency noise is properly decoupled through the capacitor and not being transferred directly from the power source to the power pin.

Figure 9 shows how to properly implement an efficient decoupling for the SR10x0's power pins.

3.2 Clock

The crystal circuit is noise sensitive and should be isolated from noise sources. Crystal circuit components should be placed as close as possible to the SR10x0. Minimizing the length of those traces will help reduce parasitic capacitance, inductance, and interference from other sources when routing these components. Care should be taken to not to route noisy high-speed digital signals close to these components or directly below them on an inner PCB layer.

A good quality uncut ground plane should be placed on the PCB layer directly under these components to provide a low impedance return path. The ground plane will also acts as a shield that protects them against noise radiated from other sources on the other side of the board (if 4 or more PCB layers are used). Similarly, making the loop area minimal is very important for the PLL filter.

Figure 9 shows a proper PCB layout for the PLL filter and the crystal oscillator components.

3.3 SPI

As the SPI interface can operate at frequencies up to 50 MHz, rising and falling edges of the clock and data signals tend to be of very short duration. Rigorous signal integrity PCB layout rules should be used for a reliable data transfer on the SPI bus. The following guidelines should be considered when a frequency higher than 10MHz is implemented.

SPI trace length should be kept as short as possible. If a length longer than 20cm need to be implemented, the line propagation delay has to be considered. The trace length of the MOSI signal should match the SCK signal trace length, in order to keep the propagation delay the same between the clock and the outgoing data line. However, we recommend routing the MISO signal with the shortest length possible, to reduce the propagation delay of the return trace to the host controller, which results in a better margin for data integrity.

Fast SPI Mode

There is a “Fast SPI” mode available in SR10x0 chips which will help reduce the propagation delay on MISO signal, and thus allow designers to implement longer SPI trace lengths.

To enable this mode, the `STDSPI` bit of the **0x0E** register should be set to 0 while the SPI speed is set lower than 10MHz. Contact SPARK Microsystems for more details.

SPI signals should be routed using controlled impedance traces with a constant impedance across the path. If possible, match the impedance of the trace to the impedance of the driver. Try to minimize the use of vias when routing these signals to reduce PCB trace impedance discontinuities that would create signal reflections. If a cable is used to connect the SR10x0 and the host controller’s SPI interface, extra care should be taken to apply the proper signal integrity rules.

Crosstalk should also be minimized on SPI signals. In order to do so, try to keep 3 to 4 times the dielectric height as spacing between the SPI traces. Adding ground shapes between the signals will also significantly reduce the crosstalk.

3.4 RF

It is important to use transmission lines with controlled impedances when designing the RF signal path on the PCB. PCB manufacturers can provide more information on how to properly implement controlled impedance transmission lines based on the PCB stack-up and materials used. There are also various impedance calculator tools available online as well.

It is also very important that an unbroken ground plane be placed underneath the RF signal path at the immediate next copper layer beneath the RF layer. For more information regarding RF transmission lines, please read section 4.3.

3.5 General PCB Stack-Up Guidelines

In this section, we will discuss PCB stack-up options.

SPARK Microsystems Antennas

Detailed information about how the PCB stack-up affects antenna design can be found in section 5.1.

Selection of number of PCB layers when designing an RF circuit is an important parameter. Too few copper layers may make it very difficult or even impossible to design a PCB that follows the impedance matching and other design guidelines. It is important to use impedance control in the design and manufacturing process of the PCB as the RF transmission lines and filter / antenna design is highly dependent on the impedance of traces. A proper geometry is required for transmission lines, and the geometry is highly dependent on the dielectric material, trace width, vertical distance between planes, and a solid ground plane of sufficient width.

RF traces use 100Ω differential or 50Ω single-ended transmission lines to minimize mismatch losses and reflections. Table 10 compares the width of these transmission lines for a 2-layer and 4-layer PCB. The table shows that the traces are much wider on a 2-layer PCB than a 4-layer PCB. On the 2-layer PCB, such a wide trace will cause an impedance mismatch when connecting to a small component pad.

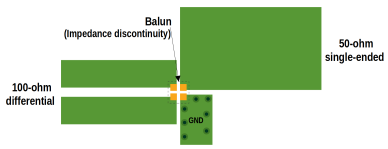
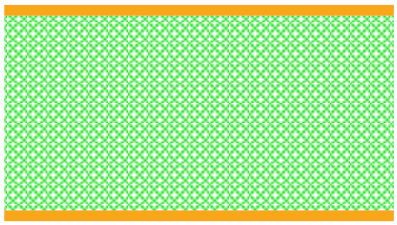
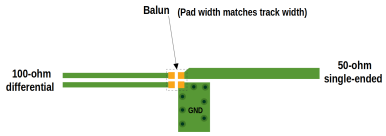
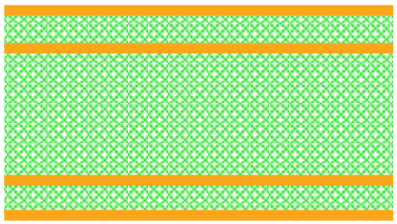
2-Layer PCB		
4-Layer PCB		

Table 10: An example of RF transmission lines on 2-layer and 4-layer stack-ups and comparison between the track widths

A 4-layer stack-up also helps with having an unbroken ground plane underneath the signal layer. By assigning the inner copper layer right beneath the component/RF-signal layer to ground, one can ensure that the RF signals maintain the shortest return paths possible. The uncut ground plane in a 4-layer PCB also helps with efficient capacitor decoupling, as these capacitors should have the shortest return current path possible to the chip. If another track cuts this return path, it will increase the return path's impedance and thus lower its noise decoupling efficiency. Furthermore, by assigning the 2nd inner layer to power planes, decoupling capacitors could be connected to a low impedance power source anywhere on the PCB which facilitates their placement as close as possible to the power pins of the chips.

An uncut inner ground plane also acts as a shield and can protect sensitive signals or components (such as crystals oscillator and PLL filter) from noisy signals (such as high-speed digital signals or noisy power traces) that are routed underneath them.

4 RF Design Guidelines

The SR10x0 can support two antenna configurations, a single-ended antenna and a differential antenna. The RF front-end will be slightly different.

4.1 Single Ended Output Design

4.1.1 Block Diagram

The RF front-end for single ended output consists of a transmission line, a balun and a monopole antenna.

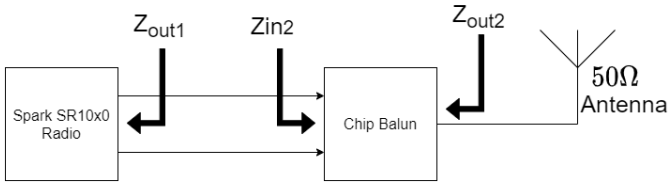


Figure 11: Block diagram of the RF front-end

Performance is optimized when the following requirements are met:

- Impedance matching between the RF front-end and the SR10x0
- Maximized radiation efficiency
- Minimized peak realized gain variation over frequency
- Maximize radiation pattern omnidirectionality

The first two requirements will be discussed in this document.

4.1.2 Impedance Matching

Maximum power will be received by providing wideband matching between the SR10x0 and the RF front-end. The input impedance of the balun (i.e. Z_{in2}) is usually matched to a balanced 100Ω. However, the output impedance of the SR10x0 (i.e. Z_{out1}) is not exactly a balanced 100Ω.

In order to minimize losses due to impedance mismatch, it is recommended to use the SR10x0 S-parameter (S2P) files (provided by SPARK Microsystems) and those provided by the balun manufacturer to tune the interconnecting transmission line for optimal impedance matching.

4.1.3 Maximum Efficiency

Due to the high frequency operation of UWB radio systems, any loss should be minimized as much as possible in the RF front-end. These losses include the return loss, insertion loss, transmission line losses (dielectric and ohmic losses).

Insertion loss and bandwidth are the most important factors to consider when chosing a chipset or PCB balun. SPARK microsystems suggests the Anaren (BD60120N50100AHF) for the SR1020 and the TDK (HHM1595A1) for the SR1010.

Moreover, the antenna should have a high radiation efficiency of above 80% over the whole frequency band of interest.

4.2 Differential Output

4.2.1 Block Diagram

The RF front-end for a differential antenna system consists of a feed line and a balanced antenna.

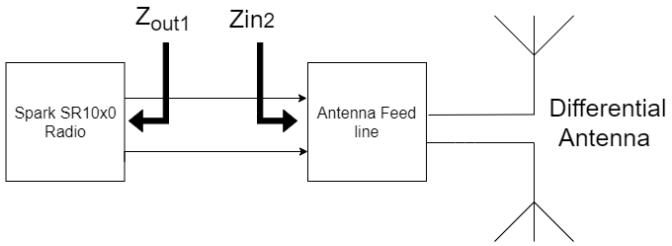


Figure 12: Block diagram of the differential RF front-end.

Performance is optimized when the following requirements are met:

- Impedance matching between the RF front-end and the SR10x0
- Maximized radiation efficiency
- Minimized peak realized gain variation over frequency
- Maximum peak gain of 4.5 dBi

The first two requirements will be discussed in this document.

4.2.2 Impedance Matching

Maximum power will be received by providing wideband matching between the SR10x0 and the RF front-end. The output impedance of the SR10x0 radio chipset (i.e. Z_{out1}) is not exactly a balanced 100Ω. However, connecting a 100Ω differential antenna may still result in acceptable performance.

In order to fully optimize the RF front-end in terms of impedance matching, it is recommended to use the SR10x0 S-parameter (S2P) files (provided by SPARK Microsystems) to tune the differential transmission line so that the impedance observed from the output of the feed line matches that of the antenna.

4.2.3 Maximum Efficiency

Due to the high frequency operation of UWB radio systems, any loss should be minimized as much as possible in the RF front-end. These losses include the return loss, radiation losses, and transmission line losses (dielectric and ohmic losses). The antenna feedline should be designed as short as possible and transmission line bends should be avoided to minimize such losses.

Moreover, the antenna should have a high radiation efficiency of above 80% over the whole UWB frequency band of interest.

4.3 RF Transmission Lines

High frequency transmission line design is optimized when the following guidelines are followed:

- The dimensions (width/length) of the RF transmission lines should be controlled based on the dielectric constant and the PCB stack-up.
- The RF transmission line should be deployed on the same layer as the SR10x0 radio chip. Using vias in the RF path should be avoided as they would cause an impedance discontinuity.
- The soldermask should be removed above the transmission lines to minimize loss and impedance change.
- Minimize insertion loss by keeping the tracks as short as possible.
- Bends with 90° angle on the transmission line should be avoided as it will result in radiation and add unwanted reflections. Instead, curved transmission lines with a large radius (Min radius = width of the trace) should be used if needed as demonstrated in Figures 13 and 14.
- For coplanar waveguide traces, use as many vias as possible near the tracks and place them as close as possible to the gap between the trace and ground plane.

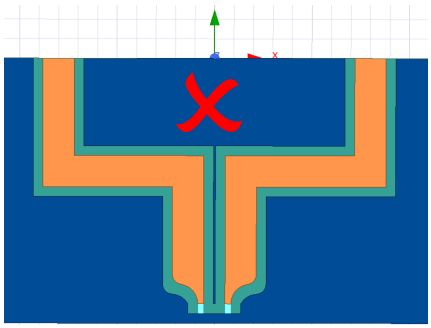


Figure 13: 90° bended track.

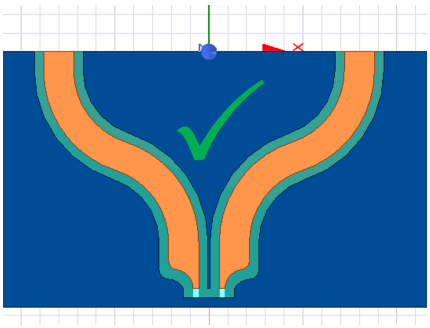


Figure 14: Curved bended track.

5 Antennas and RF Connectors

The UWB antenna needs to be placed away from the copper layers of the PCB and other components. This means that the best place for the antenna and the RF circuitry is usually at one end of the PCB. The recommended placement for I/O and power terminals is as far away as possible from the antenna, as leads and wires to these terminals can act as antennas. It is also worth noting that if other wireless technologies are being used, their antennas should not share the same area as the UWB antenna, and should be placed away from it.

That being said, we do not recommend inserting a RF connector (for cabled testing) in this area either. If you want to perform cabled testing instead of wireless testing, we strongly recommend a second PCB version with a RF connector in place of the antenna. Be sure that the RF connector and cable meet the frequency requirements of this application.

For more information regarding antenna designs for the SR10x0 chipsets, documentation is available upon request.

5.1 Information Regarding PCB Stack-up for SPARK Microsystems Antenna Designs

To help with system integration, SPARK Microsystems has developped and tested stripline antennas, which are available upon request. Unless otherwise indicated, the required PCB stack-up for those antennas should have a thickness of 0.8mm and use a 2-layer copper stack-up, as shown in Figure 15.

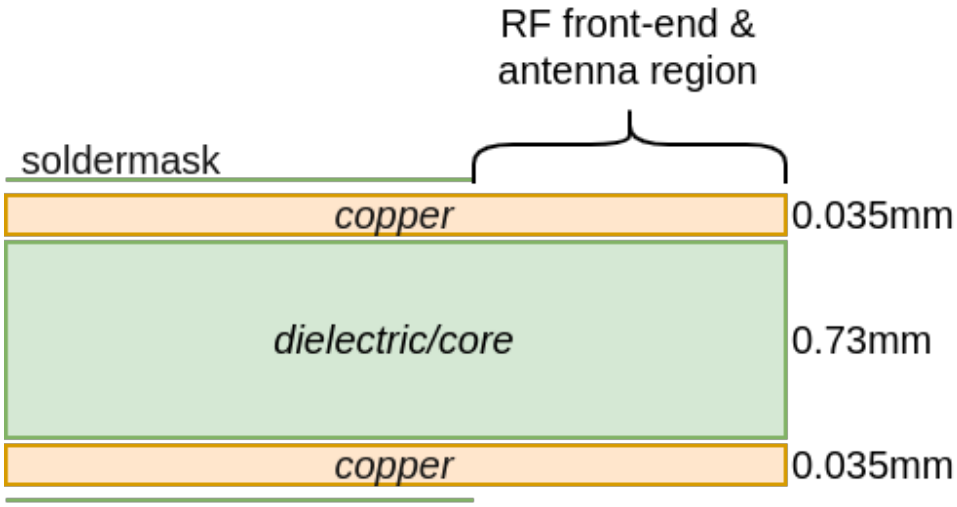


Figure 15: Required 0.8mm / 2-layer stack-up to be used with SPARK Microsystems stripline antennas

Note

All thickness values listed in this section are nominal values, ±10% tolerance is acceptable.

For applications that require a 0.8mm / **4-layer** stack-up, SPARK Microsystems antennas should be implemented as follow:

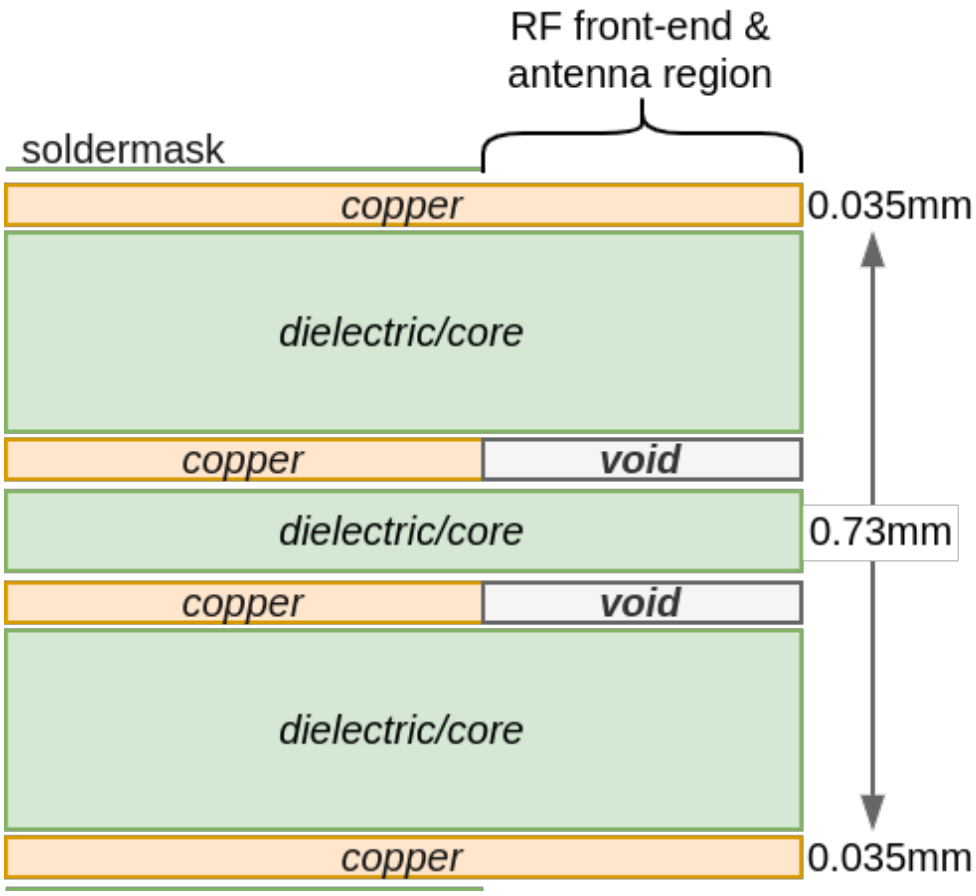


Figure 16: Recommended 0.8mm / 4-layer stack-up to be used with SPARK Microsystems stripline antennas

SPARK Microsystems stripline antennas were designed and validated using a stack-up thickness of 0.8mm. Changing that dimension to accommodate other PCB stack-ups can **negatively** impact performance. Instead, SPARK Microsystems recommends two options:

1. Relocate both the radio and the antenna on a 0.8mm thick PCB which can be connected to the main board.
2. Use a custom 4-layers stack-up on which outer layer and directly underneath inner layer are separated by a 0.73mm thick dielectric.

For the second option, Figure 17 shows an example of implementation of a recommended 1.6mm / 4-layer PCB stack-up.

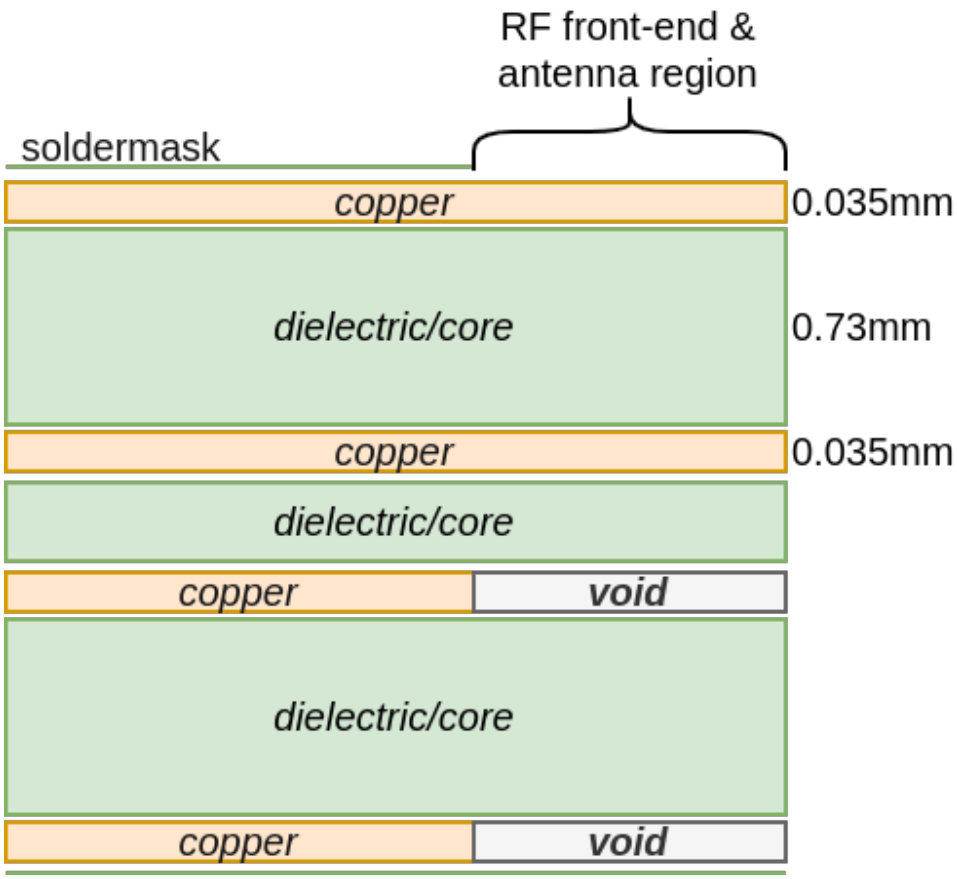


Figure 17: Recommended 1.6mm / 4-layer stack-up to be used with SPARK Microsystems stripline antennas

6 EMC/EMI Considerations

Electromagnetic Interferences (EMI) can degrade the performance of the SR10x0 radio chipset. The board designer should make sure:

- Near-by signals are not routed over split reference planes
- High-frequency signals always have a ground reference plane
- All current loops are as small as possible
- Keep low-inductance paths for decoupling and keep ceramic capacitors close to power pins
- Use ground planes on all layers of the PCB and shield internal traces with plenty of stitching vias.

Given the SR10x0 radio uses a high-speed SPI interface for its communication with the host controller, the designer should be aware of the potential EMC implication using such interface.

In order to reduce the impact on the radiated spectrum and develop towards EMC compliance, we detail a couple of well-known mitigation techniques.

6.1 Reduce System Operating Voltage

The first technique, if the system allows, is to reduce the operating voltage of both the host controller and the radio. Not only the overall power consumption of the system would be lower but also the electromagnetic emissions of the SPI interface. Designer should ensure the host controller can be operated at lower voltage, as well as ensure the SPI interface characteristics remain the same.

The radiated power contained in the signal fundamental and its harmonics is directly linked to the voltage delta of the signal. Lowering the voltage delta lowers the power, as shown in Figure 18.

WARNING

Independently lowering the operating voltage of either the host controller or the radio would result in **non-functional** SPI interface. Ensure that the operating voltage is lowered on **both devices**.

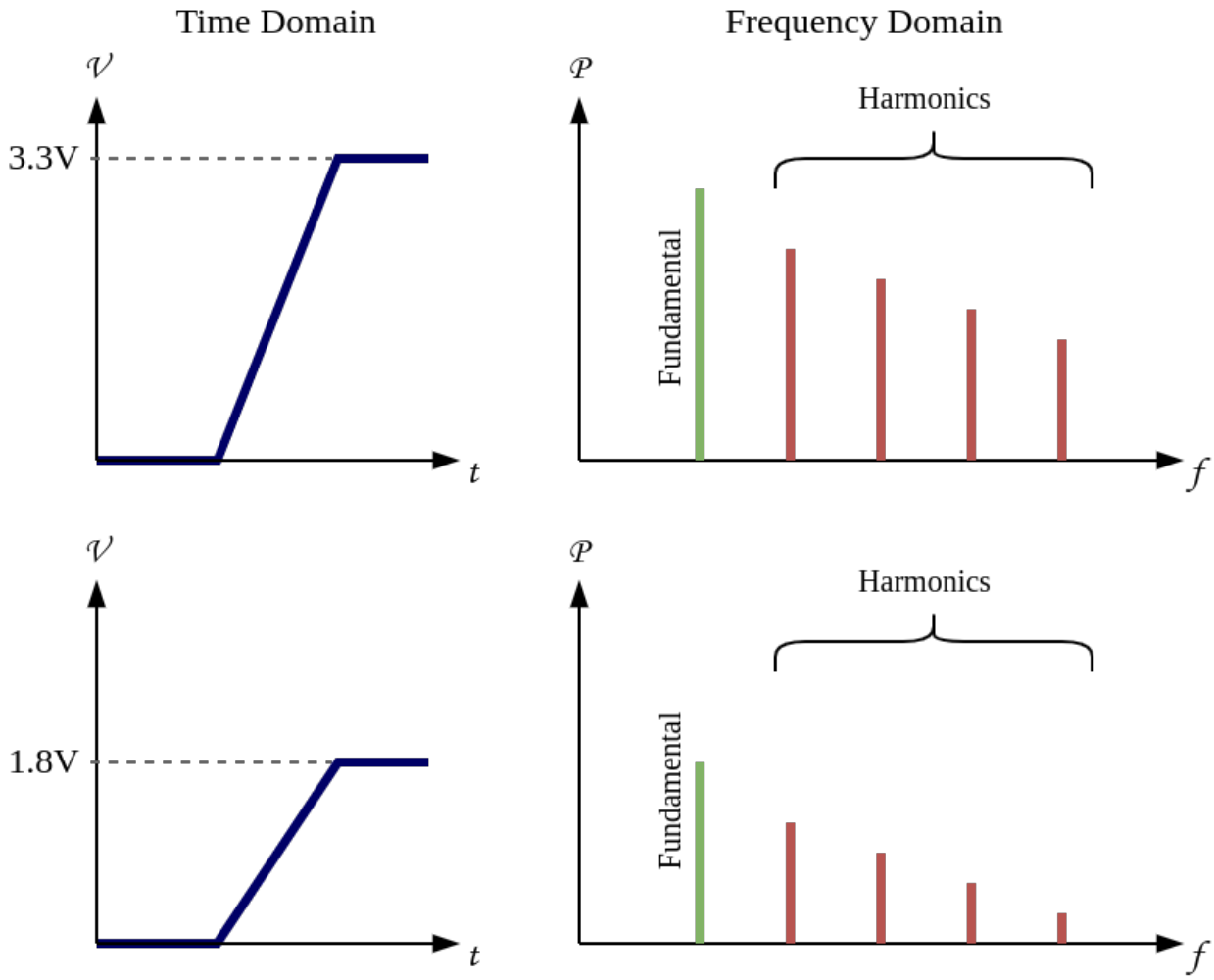


Figure 18: Impact of lowering voltage on radiated power

6.2 Reduce Speed of Edges

The second method is to reduce the speed of the signals edges, for both clock and data lines. Most host controller offer to reduce the speed of its SPI interface edges, and it usually controls both rising and falling edges of the signal being transmitted.

The frequency content of a signal is directly related to its shape. A square wave contains many harmonics of the fundamental frequency of the signal. Reducing the speed of the edge reduces the frequency content of the signal and therefore the radiated power of its harmonics, as shown in Figure 19.

WARNING

The designer should ensure that the SPI interface still operates in accordance to the standard. ”Degrading” the signal edges can cause the SPI interface to be inoperable, creating data corruption due to timing constraint being shifted using this technique.

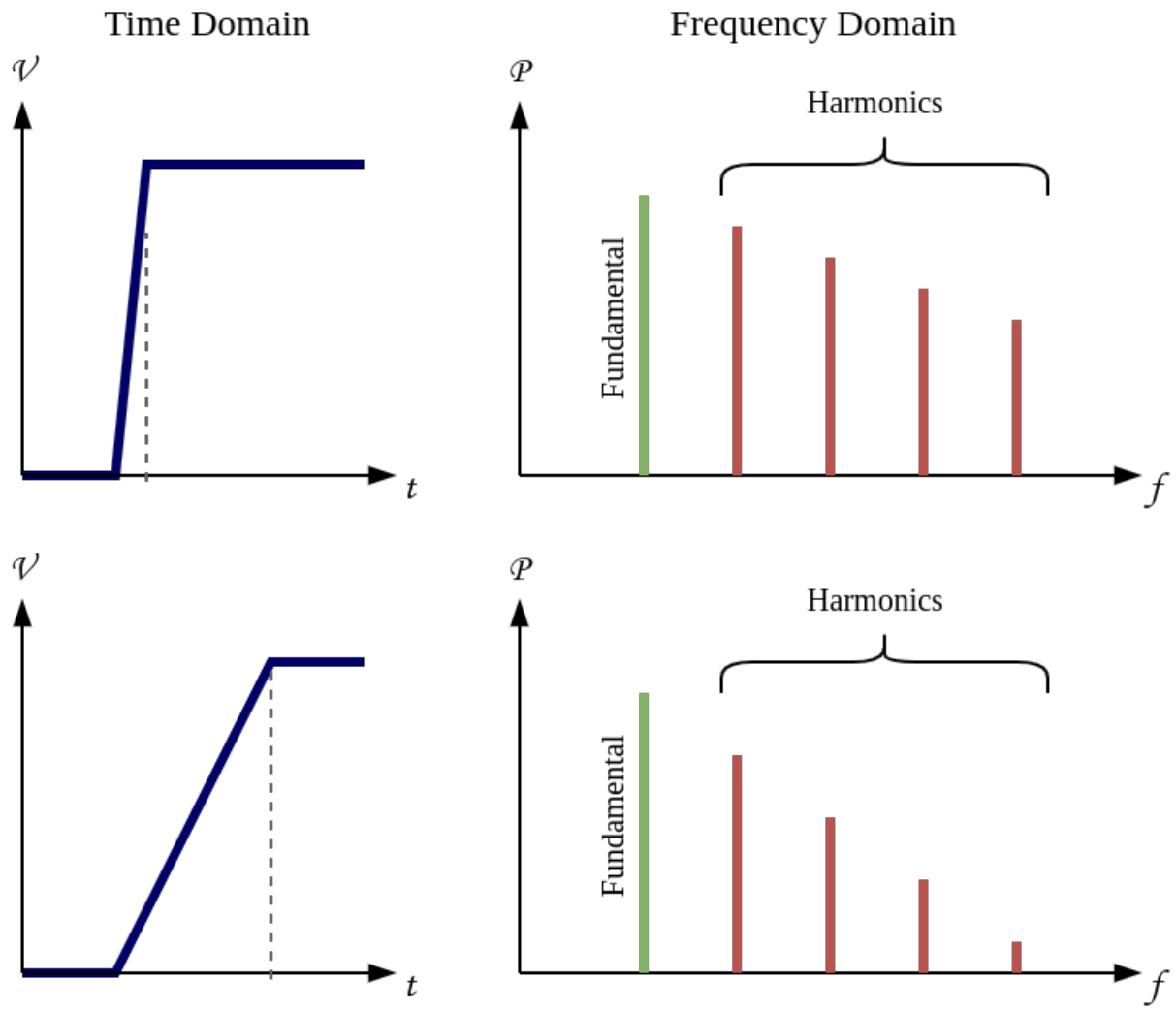


Figure 19: Impact of slowing down edges on radiated power

7 Revisions

Revision	Changes
1.2	Added new sections, multiple corrections and improvements
1.1	Formatting and figures update, multiple text corrections and improvements
1.0	Initial Release

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